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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/030,834	01/10/2002	Charles Bailey Neal	RCA 89633	2357

7590

05/17/2006

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EXAMINER
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TRAN, TRANG U

ART UNIT	PAPER NUMBER
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2622

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/030,834

Applicant(s)

NEAL, CHARLES BAILEY

Examiner

Trang U. Tran

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed Feb. 23, 2006 have been fully considered but they are not persuasive.

In re pages 5-8, applicant states that the examiner's interpretation of the term OSD is improper with respect to the present claims in view of the specification and the understating of those skilled in the art; however, in order to move the prosecution of this case forward, applicant has amended claims 1 and 6 to more clearly and distinctly claim the subject matter that applicant regards as his invention and argues that nowhere does Han teach or suggest OSD generating means capable of providing OSD signals in any one of a plurality of color formats and nowhere does Han teach or suggest generating OSD signals in accordance with a selected one of the first and second color format that corresponds to a color format associated with the selected video signal.

In response, the examiner respectfully disagrees. First at all, since claims 1 and 6 have been amended to more clearly and distinctly claim the subject matter that applicant regards as his invention, the interpretation of the term OSD in the last Office Action is considered to be moot.

Finally, Han discloses in col. 2, lines 11-15 that

**"FIG: 1 shows a preferred embodiment of a HDTV video processor according to the present invention including a data receiver 1 processing and outputting a digital TV (DTV) video data, NTSC or VGA video data having different color formats, the format information and various control signals",**

in col. 3, lines 11-19 that

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“As shown in FIG. 3, the OSD processor 15 also further includes a data converter 151 which receives and converts the OSD data output from the memory interface 13 into a uniform format and output from the memory interfacier 13 into a uniform format and outputs a control signal to output the data in the selected OSD receiver; and a multiplexer (MUX) 153 **which overlays the converted data from the format converter 14 with the OSD data output from the data converter 151 according to the control signal from the data converter 151**”,

in col. 4, lines 27-36 that

“The format converter 14 receives the DTV or the NTSC/VGA video data through the memory interfacier 13 and converts the input format of the data to the designated output format according to the display and video format output by the host interfacier 112. Specifically, the format converter 14 receives the DTV or NTSC/VGA video data having a YCbCr color format of 4:4:4, 4:2:2, or 4:2:0 and outputs a converted video data having a uniform YCbCr color format of 4:4:4”, and

in col. 4, lines 37-48 that

“The OSD processor 15 receives the converted data from the format converter 14 and overlays both the DTV or NTSC/VGA images with the OSD data stored in the memory 12. As shown in FIG. 3, the **data converter 151 outputs the memory access signal to the memory interfacier 13 and reads the OSD data stored in the memory 12. The data converter 151 converts the read OSD data having a YCbCr color format of 4:4:4, 4:2:2, or 4:2:0 into one uniform YCbCr color format of 4:4:4 and outputs the converted data to the MUX 153 for outputting the OSD data to the OSD location**”.

From the above messages, it is clear that the data receiver 1 of Han can select one of the first and second video signal sources (DTV or NTSC/VGA) and provides a selected video signal for processing, the video being representative of a video program and formatted in accordance with one of a first color signal format and a second color signal format (4:4:4, 4:2:2, or 4:2:0) as recited in the amended claims 1 and 6 and the data converter 151 of Han generates an On Screen Display (OSD) signal for forming a graphics display that is overlaid onto one of the first and second video programs, the

data converter 151 capable of providing the OSD signal in any one of the first and second color formats, wherein the generated OSD signal is formatted in accordance with a selected one of the first and second color format that corresponds to a color format associated with the selected video signal as recited in the amended claims 1 and 6. Thus, the claimed OSD generating means recited in amended claim 1 and corresponding steps recited in amended claim 6 are anticipated by the data converter 151 of Han.

In re page 8, applicant states, with respect to claim 3, that Susumu Imai is cited as teaching a conversion matrix for converting R, G, B components into Y, I, Q components and; however, such a teaching fails to cure the defect of Han and Fujimoto as applied to claim 1 discussed above.

In response, as discussed above with respect to claim 1, Han does indeed disclose the claimed OSD generating means.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-2 and 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han (US Patent No. 6,421,094 B1) in view of Fujimoto (US Patent No. 5,912,710).

In considering claim 1, Han discloses all the claimed subject matter, note 1) the claimed a video signal processing apparatus (Figs. 1 and 2), comprising: a first video

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signal representative of a first video program and formatted according to a first color format is met by the NTSC or VGA video data which have the format information on each respective video data and various control signals (Figs. 1-2, col. 2, line 11-43 and col. 3, lines 47-63), 2) the claimed a second video signal source for providing a second video signal representative of a second video program and formatted according to a second color format is met by the DTV video data which has different color formats (Figs. 1-2, col. 2, lines 11-43 and col. 3, lines 37-47), 3) the claimed switch means that selects one of the first and second video signal sources and provides a selected video signal for processing is met by the memory interfacer 13 which selects the video data output from the data receiver and managing the writing/reading of the selected data on/from the memory 12 (Figs. 1-2, col. 2, lines 11-46 and col. 3, lines 47-63), 4) the claimed means for generating an On Screen Display (OSD) signal for forming a graphics display that is overlaid onto one of the first and second video programs, the generating means capable of providing the OSD signal in any one of the first and second color formats, wherein the generated OSD signal is formatted in accordance with a selected one of the first or second color format that corresponds to a color format associated with the selected video signal is met by the OSD processor 14 which further includes a data converter 252 which receives and converts the OSD data output from the memory interfacer 13 into a uniform format and outputs a control signal to output the data in the selected OSD receiver (Figs. 1 and 3, col. 3, line 5 to col. 4, line 55), 4) the claimed a plurality of color conversion matrices for converting the color information in the color palette to provide the OSD signal, which is formatted in accordance with the

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selected one of the first or second color format is met by the data converter 151 which converts the read OSD data having a YCbCr color format of 4:4:4, 4:2:2, or 4:2:0 into one uniform YCbCr color format of 4:4:4 and outputs the converted data to the MUX 153 (Figs. 1-3, col. 3, line 5 to col. 4, line 55), and 5) the claimed means operatively coupled to the OSD generating means and the first and second video signal sources, for combining the OSD signal generated by the OSD generating means with the selected one of the first or second video signals is met by the multiplexer (MUX) 153 which receives the converted OSD data from the data converter 151 and the converted DTV or NTSC/VGA data from the format converter 14 according to the control signal from the data converter 151 (Figs. 1-3, col. 3, line 5 to col. 4, line 55).

However, Han explicitly does not disclose the claimed the generating means comprising a color palette that includes color information formatted in accordance with a predetermined color format.

Fujimoto teaches that the RGB color palette circuit 104a converts the pixel data to RGB color data, for example, when one pixel of the graphics data is comprised of an index color mode having eight bits/pixel, the index color data are converted to a color data of twenty-four bits for the respective colors of R (red), G (green) and B (blue) (Fig. 1, col. 7, lines 1-23).

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the RGB color palette as taught by Fujimoto into Han' s system in order to optimize the hardware for an OSD data processing in converting data of various color formats and OSD formats into a uniform format.

In considering claim 2, the claimed wherein the color palette comprises color information formatted in the RGB format is met by the RGB color palette circuit 104a converts the pixel data to RGB color data (Fig. 1, col. 7, lines 1-23 of Fujimoto).

In considering claim 4, the claimed wherein the first video signal is an analog television signal is met by the NTSC or VGA video data which have the format information on each respective video data and various control signals (Figs. 1-2, col. 2, line 11-43 and col. 3, lines 47-63).

In considering claim 5, the claimed wherein the second video signal is a digital television signal is met by the DTV video data which has different color formats (Figs. 1-2, col. 2, lines 11-43 and col. 3, lines 37-47).

In considering claim 6, Han discloses all the claimed subject matter, note 1) the claimed a method of producing graphics having a color format that matches the color format of a received signal, the method comprising the steps of: selecting a video signal source from a plurality of video signal sources to provide a selected video signal, the video being representative of a video program and formatted in accordance with one of a first color signal format and a second color signal format is met by the data receiver 11 which receives and outputs a DTV video data, an NTSC or VGA video data, an OSD data and the memory interfacier 13 which selects the video data output from the data receiver and managing the writing/reading of the selected data on/from the memory 12 (Fig. 2, col. 2, line 38 to col. 3, line 10), 2) the claimed providing a plurality of color conversion matrices, wherein each color conversion matrix is adapted to convert the color information in the color palette to provide a graphics signal that is formatted in



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accordance with a particular color format, wherein said plurality of color conversion matrices enables providing graphics signals in any one of the first and second color formats is met by the data converter 151 which converts the read OSD data having a YCbCr color format of 4:4:4, 4:2:2, or 4:2:0 into one uniform YCbCr color format of 4:4:4 and outputs the converted data to the MUX 153 (Figs. 1-3, col. 3, line 5 to col. 4, line 55), 3) the claimed selecting a desired one of the plurality of color conversion matrices that corresponds to the selected video signal source and generating a graphics signal for forming a graphics display that is overlaid onto the video programs, the graphics signal being formatted in accordance with one of the first color signal format and the second color signal format that corresponds to a color format associated with the selected video signal is met by the host interfacer 112 which receives the DTV video format information from the frame controller 11, the NTSC and VGA mode signal and the host interface signal, and outputting an OSD data, display format information, input format information, and various control signals to select the desired one of the plurality of color conversion matrices (Fig. 2, col. 2, line 63 to col. 4, line 55), 4) the claimed combining the graphics signal with the received signal is met by the multiplexer (MUX) 153 which receives the converted OSD data from the data converter 151 and the converted DTV or NTSC/VGA data from the format converter 14 according to the control signal from the data converter 151 (Figs. 1-3, col. 3, line 5 to col. 4, line 55), and 5) the claimed processing the combined signal to generate an output signal is met by the color space converter 16, a Look Up Table (LUT) 17 further processing the OSD

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overlaid video data and displays on the monitor (Figs. 1-2, col. 4, line 56 to col. 5, line 23).

However, Han explicitly does not disclose the claimed providing a color palette that includes color information formatted in accordance with a predetermined color format.

Fujimoto teaches that the RGB color palette circuit 104a converts the pixel data to RGB color data, for example, when one pixel of the graphics data is comprised of an index color mode having eight bits/pixel, the index color data are converted to a color data of twenty-four bits for the respective colors of R (red), G (green) and B (blue) (Fig. 1, col. 7, lines 1-23).

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the RGB color palette as taught by Fujimoto into Han's system in order to optimize the hardware for an OSD data processing in converting data of various color formats and OSD formats into a uniform format.

In considering claim 7, the claimed wherein the color palette comprises color information formatted in the RGB format is met by the RGB color palette circuit 104a converts the pixel data to RGB color data (Fig. 1, col. 7, lines 1-23 of Fujimoto).

In considering claim 8, the claimed wherein the color conversion matrices convert the color information in the color palette into one of a Y, PR, PB formatted signal and Y, PI, PQ formatted signal is met by the color space converter 104b which converts the RGB color data from the color palette circuit 104a to YCrCb television standard (Fig. 1, col. 7, lines 1-23 of Fujimoto).

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Han (US Patent No. 6,421,094 B1) in view of Fujimoto (US Patent No. 5,912,710), as applied to claim 1 above, and further in view of Susumu Imai (JP 403268594 A (see abstract)).

In considering claim 3, the claimed wherein the plurality of conversion matrices includes a conversion matrix for converting the color information in the color palette into Y, PR, PB format is met by the color space converter 104b which converts the RGB color data from the color palette circuit 104a to YCrCb television standard (Fig. 1, col. 7, lines 1-23 of Fujimoto).

However, the combination of Han and Fujimoto explicitly do not disclose the claimed a conversion matrix for converting the color information in the color palette into Y, PI, PQ format.

Susumu Imai teaches that in an picture recoding system, an RGB-YIQ conversion part 2 executes the matrix conversion of a digital signal consisting of R, G and B components into a brightness component Y and color difference components I, Q and sends the converted components Y, I, Q to a digital recording part 5 (see abstract).

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the RGB-YIQ matrix conversion as taught by Susumu Imai into the combination of Han and Fujimoto's system in order to attain partial emphasis corresponding to human visual sense without damaging a gradation change by converting digital picture into a brightness component and color difference components (see abstract of Susumu).

***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trang U. Tran whose telephone number is (571) 272-7358. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TT  
May 10, 2006



Trang U. Tran  
Examiner  
Art Unit 2622